

# SiliconBurmuin: A Horizon Europe propelled Neurocomputing Initiative in the Basque Country

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**Abstract**—SiliconBurmuin is aimed at creating a multi-disciplinary neurocomputing community in the Basque Country, bringing together technology and scientific research centres and industry companies. This community will: (1) identify key biological structures and mechanisms that play a major role in vision across species, and (2) transform this knowledge into novel mathematical formalisms, neuromorphic designs and algorithms to solve industry challenges and enable new experiments of interest in neuroscience and clinical research. To achieve the latter objective in a time-effective manner, SiliconBurmuin will draw strong connections with the ongoing Horizon Europe NimbleAI project, with which it shares coordination. This is expected to allow reinforcement of ideas, knowledge and technology via a common prototyping platform where to implement IP from both projects. In addition to describing the research objectives and direction of SiliconBurmuin, this paper posits that co-ordination and co-funding of aligned projects at EU and regional levels might well be a catalyst for raising regional self-awareness of own potential and develop it to help fulfill global challenges, such as semiconductor sovereignty.

## I. INTRODUCTION

Neuromorphic technology takes inspiration from biological sensory perception to design extremely energy-efficient and low-latency event-driven semiconductor devices that outperform decades-old von Neumann processors [1]. After a period of steady development, neuromorphic technology is now considered a ‘critical enabler’ by Gartner; and Yole predicts that by 2035, neuromorphic chips will serve up to 18% of the exponentially growing multi-billion dollar AI semiconductor market [2]. This potentially huge market segment is being targeted by big corporations and deep-tech startups alike, including among others: SONY, Intel, Samsung, iniVation, BrainChip, GrAI Matter Labs (GML), Synsense, Rain, SpiN-Cloud, Innatera and Prophesee. Interestingly, most of the latter startups emerged from (and continue to be strongly connected to) academic multidisciplinary environments, where

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neuroscientists, mathematicians and engineers work together to move disruptive bio-inspired concepts to semiconductor designs, and eventually deliver commercial chips [3].

Inspired by these success cases, IKERLAN has started the SiliconBurmuin\* initiative to set up one of such multidisciplinary communities in the Basque Country. It brings together the largest university in the region and six research centres with expertise in technology and scientific areas related to neuroscience, neurology, mathematics, RTL design, AI and algorithms. SiliconBurmuin is backed by the Basque Government, and is completed with the Basque Microelectronics Hub to build institutional liaison with the Spanish PERTE Chip and EU’s Chips Act. A major goal of SiliconBurmuin is to reveal and transform neuroscience knowledge into neuromorphic technology to meet the most demanding industry needs, initially targeting vision requirements of autonomous trains [4]. Current members of SiliconBurmuin are listed in Fig. 1.










<b>Coordination &amp; RTL design</b>	Ikerlan	
<b>Neuroscience</b>	Achucarro Basque Center for Neuroscience	
	Basque Center on Cognition, Brain and Language (BCBL)	
<b>Neurology</b>	IIS BioCruces Bizkaia	
<b>Mathematics</b>	Basque Center for Applied Mathematics (BCAM)	
<b>AI &amp; Algorithms</b>	Vicomtech	
<b>Academia</b>	University of the Basque Country (UPV/EHU)	
<b>Institutional liaison</b>	Basque Microelectronics Hub (BMH)	
<b>Industry use case</b>	CAF (Autonomous train)	

Fig. 1: SiliconBurmuin initiative members

SiliconBurmuin will run in tandem with the NimbleAI Horizon Europe research project, which is also coordinated by IKERLAN, and seeks to boost energy-efficiency and performance in next-generation neuromorphic vision and AI

\*Burmuin means *Brain* in Basque language

chips [5]. This is expected to help SiliconBurmuin align with commercial roadmaps and access state-of-the-art technology of NimbleAI partners: high-TRL pre-commercial IP and low-TRL testchips that implement disruptive concepts, such as digital foveation.

The article is organized as follows. Section II outlines the NimbleAI project and introduces the key concepts that SiliconBurmuin will build upon. Then, Section III explains the SiliconBurmuin initiative, detailing the undertaken approach, objectives and expected outcomes in its main axes: neuromorphic technology, neurocomputing techniques, semiconductor design, and industry links. Finally, Section IV sums up the main takeaways to conclude the paper.

## II. THE NIMBLEAI HORIZON EUROPE PROJECT

The recently started NimbleAI project leverages key principles of energy-efficient light detection in eyes and visual information processing in brains to create an integral sensing-processing neuromorphic architecture [5]. It is expected that findings coming out from this project will lead to practical implementations in next-generation commercial chips.

NimbleAI considers that processing begins in the sensor, where important efficiency gains are expected from the use of in-sensor pre-processing and novel dynamic vision sensing modes. More specifically, the project studies techniques and designs circuits to capture and optimally represent the spatiotemporal evolution of 3D visual scenes using information-rich event flows that match the optimization features implemented in the downstream processing and inference engines in the architecture. The expectation is that by investing some computing power and energy to gain some situational awareness early, a major reduction of the subsequent workload will be achieved, saving lots of energy by doing that. This is inspired by unconscious visual processing and selective attention mechanisms in eye-brain systems, in which visual processing actually begins in the retina.

To achieve this, NimbleAI is designing the world's first light-field Dynamic Vision Sensor (DVS) with digital foveation, which combines divergent evolutionary vision developments such as foveation in vertebrate eyes and compound insect eyes.

*Digital foveation* allows to dynamically allocate sensing resolution in the DVS based on the information value brought about by each image region, which is decided by selective visual attention and optical flow algorithms [6]. The final objective is to maximize the amount of meaningful information that can be captured without unnecessarily increasing the processing workload. Digital foveation mimics the foveation mechanism in vertebrate eyes, where a central foveated region is seen in greater detail (e.g., salient object) than peripheral regions (e.g., background). In the DVS, several foveated Regions of Interest (ROIs) that match the size, shape and moving dynamics of the recognized and tracked salient objects can be sensed simultaneously. A foveated DVS testchip with expected resolution of 400x400 pixels is being designed and manufactured by CSIC using X-FAB 180-nm process node.

*Event-driven light-field 3D perception* captures directional light variations with a custom-made array of microlenses by Raytrix coupled to a SONY-Prophesee IMX636 DVS [7]. This is inspired by the functioning of insect compound eyes, which allows them to accurately estimate depth and motion in a visual scene [8]. NimbleAI investigates lightweight algorithms to pair DVS events related to the same incoming light rays based on their temporal activation patterns and the microlenses geometry, as a first step to estimate the origin of those rays. This is expected to help circumvent compute-intense correlations typically required by frame-based light-field processing [9]. Light-field enabled depth estimations hold a great potential for ROI selection (e.g., nearby objects) and to improve end-to-end perception accuracy.

Along with the light-field and foveated DVS, NimbleAI is designing an end-to-end event-driven processing architecture to seamlessly run energy-efficient Spiking Neural Networks (SNNs) and user-trained industry standard Convolutional Neural Networks (CNNs). Namely, SNNs are used to power near-sensor selective visual attention engines that detect ROIs, and CNNs are used subsequently to infer visual information in the selected ROIs. Imec is designing an SNN testchip and the University of Manchester is designing the accompanying SNN algorithms to detect the ROIs. NimbleAI also explores ways to continuously improve on dynamically selecting ROIs by feeding visual inference results delivered by CNNs back to train the SNNs online. Note that SNNs are particularly well suited for online training as their learning rules typically use only information local to the synapse [10], which results in lower computational burden than backpropagation.

Recent research has shown that CNNs designed and trained with popular AI frameworks (e.g., TensorFlow) can be converted to equally accurate event-driven networks with lower computational complexity and hence greater efficiency [11]. As it occurs with SNNs, the type of events that are processed by event-driven CNNs correspond with the events delivered by the DVS. To exploit this, the NimbleAI architecture integrates an event-driven dataflow AI accelerator (i.e., GML NeuronFlow [12]). This is adapted to run multiple event-driven CNNs with varying topologies simultaneously, and thus benefit from digital foveation. The NimbleAI architecture is completed with a downstream processing engine that integrates a Codaip RISC-V CPU, Menta eFPGA fabric, and CEA CSRAM in-memory computing memory blocks [13].

NimbleAI will prototype key components of its architecture via small-scale stand-alone testchips to produce silicon-proven neuromorphic IP. As shown in Fig. 2, these testchips will be used in a prototype of the entire NimbleAI sensing-processing architecture together with other commercial neuromorphic chips, including the SONY-Prophesee IMX636 DVS and the GML GrAI VIP that implements NeuronFlow IP. The NimbleAI prototype will also include an FPGA to accommodate user RTL, and will be accompanied with the corresponding programming tools and OS drivers to enable users run their CNN models on it. SiliconBurmuin will use this prototype as a research vehicle to test novel neuromorphic IP and algorithms.

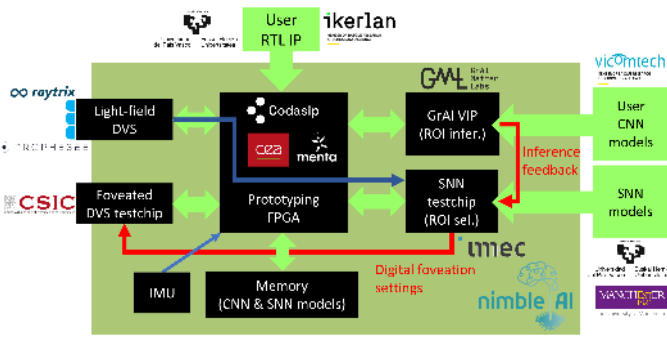


Fig. 2: NimbleAI prototype

### III. THE SILICONBURMUIN INITIATIVE

Fig. 3 shows the SiliconBurmuin members and expected relations with NimbleAI partners, which include world-leading research institutions and companies from the semiconductor and neuromorphic technology sectors. This collaborative framework is expected to help SiliconBurmuin achieve its ambitious main objectives:

- (1) Extend event-driven visual sensing and in-sensor pre-processing modes considered in NimbleAI to further optimize the use of bandwidth between the DVS and the host processor. Design event-driven algorithms and RTL logic to support these modes and demonstrate the RTL designs in silicon – going beyond the currently existing ‘glass floor’ in the Basque Country for RTL implementation that are FPGAs.
- (2) Train and characterize biologically plausible SNN-based circuits that mimic early visual perception mechanisms using adapted data analysis and modelling tools from computational neuroscience.
- (3) Optimize traditional computer vision algorithms with relevance to industry to run in state-of-the-art neuromorphic chips (especially those available in the NimbleAI prototype), and demonstrate technology advantages derived from their use in real-world scenarios (e.g., CAF autonomous train).
- (4) Find uses of neuromorphic technology in neuroscience research and clinical detection of neurocognitive diseases.
- (5) Provide a technology context to continue elaborating the Neural Automata (NA) mathematical formalism proposed by BCAM [14], and demonstrate uses of NA to design novel neuromorphic circuits.

Note that the objectives above provide interesting multidisciplinary collaboration opportunities for the SiliconBurmuin members. Achieving these objectives would result in novel RTL and algorithms being prototyped (together with other commercial-grade IP provided by NimbleAI partners) and tested in industry use cases. This is expected to help open commercialization opportunities for SiliconBurmuin outcomes (via IP licensing). Likewise, SiliconBurmuin is expected to provide traction for the development of academic environments in Basque universities (e.g., UPV/EHU) that cultivate the skillsets requested by the growing semiconductor and neuromorphic industries. The next subsections elaborate on the main axes of SiliconBurmuin.

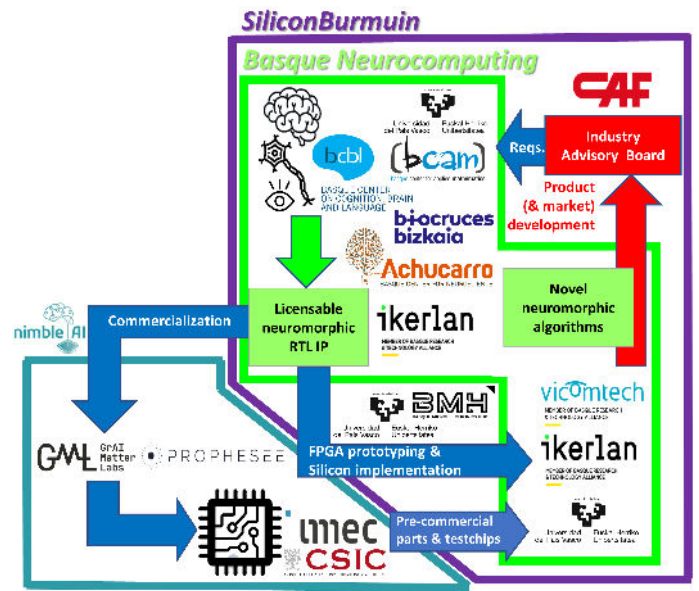


Fig. 3: SiBurmuin framework and relations with NimbleAI

#### A. Neuromorphic Axis

The main objective of this axis is to generate neuromorphic IP (RTL designs and algorithms) taking inspiration from the early stages of biological visual systems [15], [16]. As shown in Fig. 4, SiliconBurmuin seeks to: (1) increase the neuromorphic visual sensing modalities of NimbleAI, adding event-based hyperspectral vision; and (2) design sensor fusion techniques to extract and squeeze the high-value information of all acquired multimodal data into a bandwidth-limited communication channel with a host processor. The project will explore optimization opportunities enabled by context-aware DVS functioning adjustment in commercial DVS chips as well as in the NimbleAI foveated testchip. The objective is to enhance efficiency at both pixel and image region levels.

More specifically, SiliconBurmuin will look into adjusting the global brightness threshold in the SONY-Prophesee IMX636 DVS to control the visual event generation rate. Inspired by the inhibitory behaviour of neighbor bipolar neurons in the retina, the project will also investigate using local brightness thresholds for clusters of pixels [16]. Likewise, different types of spatiotemporal event filters will be explored, including those that can be tuned to the particular movement patterns and temporal dynamics perceived across sensed image regions. These can be estimated using optical flow algorithms [6], which will also be used for predicting the evolution of the visual information distribution in the scene. Note this is of utmost importance to detect and track ROIs, and hence adjust settings in the foveated DVS testchip.

Optical flow estimations will therefore help decide the optimal adjustment of the foveated regions in the NimbleAI DVS testchip as well as tune the subsequent spatiotemporal event filters. An interesting research direction is to trade off accuracy and processing burden by applying optical flow algorithms with the appropriate spatial granularity tailored to the sizes and positions of the moving objects detected in the

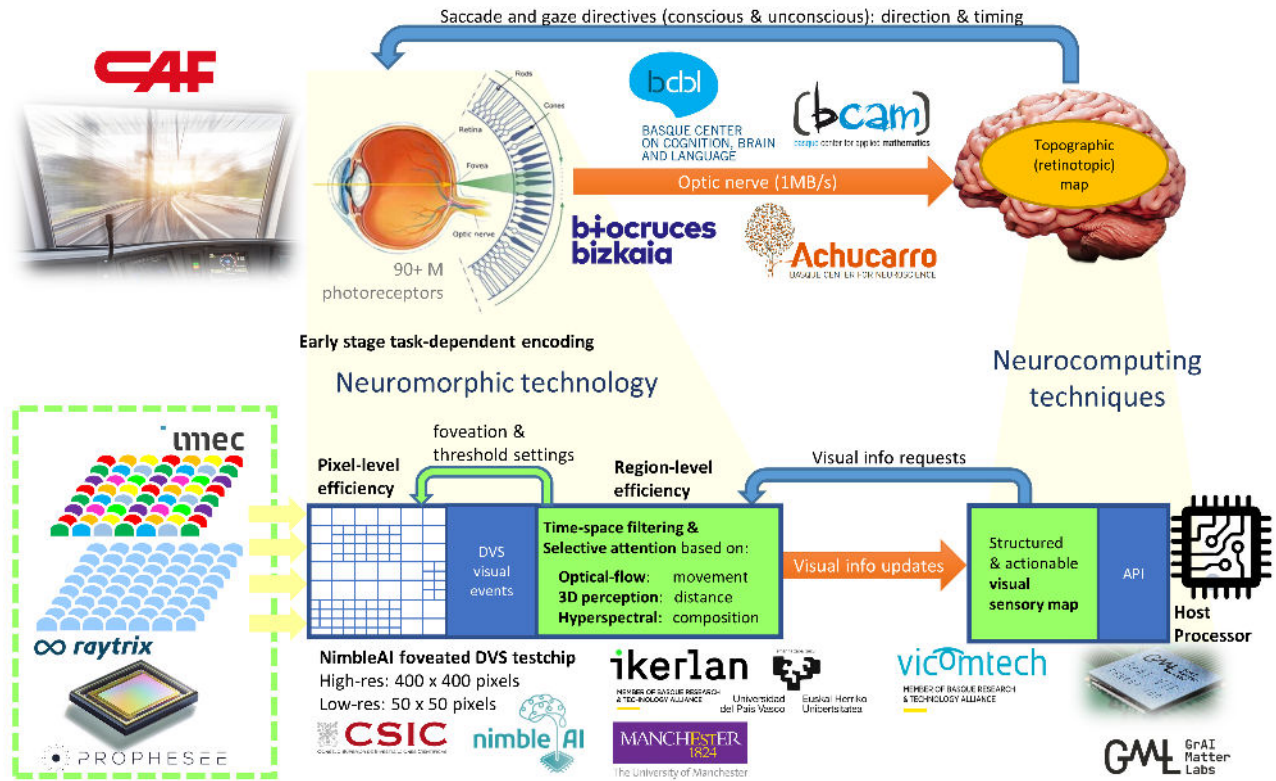


Fig. 4: Human visual system vs. SiliconBurmuin (& NimbleAI) approach

ROIs – in connection with the configured foveation settings. Another potential way to simplify optical flow algorithms might well be to integrate depth estimations delivered by light-field algorithms currently in development in NimbleAI.

SiliconBurmuin will also study whether hyperspectral DVS could result in simpler pipelines and neural networks than those used in mainstream shape-based vision. This is inspired by some stomatopod crustaceans, which have up to 16 types of photoreceptors sensitive to different spectral light bands and yet very simple visual systems [17]. In fact, hyperspectral vision has already been proven to cope well with metamerism, overlapping objects, background clutter, as well as adverse weather conditions such as rain and fog [18].

SiliconBurmuin will study the feasibility of combining Imec’s Fabry-Perot on-chip optical filters [19] and DVS technologies to enable event-driven hyperspectral vision. Namely, the project will investigate opportunities to exploit advantages brought about by DVS sensors, including the NimbleAI foveated testchip, and identify limitations imposed by the combination of Imec’s Fabry-Perot optical filters and DVS technologies in terms of the number, width and location of spectral bands. It will also generate limitation-aware event-based hyperspectral datasets using data acquired with the SONY-Prophesee IMX636 DVS onboard CAF trains operating in real life (see subsection III.D).

Eventually, SiliconBurmuin will seek to co-design multi-modal event-driven algorithms and RTL logic that operate in a spatiotemporal mode (e.g., SNN-based circuits) to fuse DVS, light-field and hyperspectral data and thus improve visual

scene recognition by discerning objects based on their 3D position, chemical composition and shape.

Expected outcomes of this axis include: (1) the world’s first hyperspectral DVS technology feasibility study and associated datasets; (2) event-driven optical flow algorithms that integrate depth information; and (3) RTL designs to dynamically adjust settings in foveated DVS sensors to work at the optimal point and fuse event-based multimodal data.

### B. Neurocomputing Axis

As shown in Fig. 4, visual information acquired by the retina is integrated into the brain cortex to compose a topographic (retinotopic), hierarchical and actionable map of the surroundings (exteroception), which also includes representations of body parts (proprioception) [16], [20]. The relations between proprioception and exteroception representations in the topographic map play an important role in selecting attentional targets and coordinating physical interactions with the environment, such as sensorimotor behaviors.

One major objective of this axis is to build an API inspired by the topographic mapping of the retina in the brain, and hence provide user applications with visual perception information via actionable access to the multimodal neuromorphic vision system discussed in subsection III.A. Following neuroscience principles, SiliconBurmuin will be looking to enable proprioception-exteroception interactions in the API-accessible topographic visual map, exploring ways to represent ego-motion information and processing resources available in the host processor at each time.

This axis also envisions two experiments that require collaboration among neuroscientists, clinical researchers and engineers to combinely use neuromorphic technologies (i.e., DVS and SNN) and neurocomputing techniques.

In the first experiment, SNNs oriented to visual processing will be trained with experimental visual cortex datasets from humans and animals engaged in visual scene recognition. NimbleAI will seek to adapt modelling techniques commonly used in computational neuroscience for use with SNNs, which are orders of magnitude simpler and smaller than biological network counterparts, yet work at notable higher speeds. The objective is to detect and characterize interesting behavior patterns in SNNs that are similar to behaviors recorded using functional magnetic resonance (i.e., macro level: network outputs) and/or responses of neurons in visual pathways recorded in awake animals (i.e., micro-level: activations of SNN neurons).

For example, spatiotemporal activation patterns of neurons that remain similar across SNNs trained with different visual contexts could indicate an inherent mechanism to direct processing of other SNN parts towards image regions with potentially valuable early-stage information (i.e., ROIs). This could play an important role in building generalizable ROI selection engines, at least for a wide range of visual contexts. Selected ROIs could then be processed with CNN-based powerful computer vision solutions created with popular AI frameworks, instead of other SNN parts. Note this is the same objective pursued in NimbleAI, but approached from a complementary neuroscience perspective.

In a second experiment, the number and properties of visual events delivered by a SONY-Prophesee IMX636 DVS will be used to measure the complexity of visual scenes. Different statistical modeling techniques typically used to characterize data patterns in computational neuroscience will be applied; e.g., point-process, independent components or avalanches. The aim of the experiment is to characterize the perception abilities of healthy subjects and patients with neurocognitive diseases (e.g., Alzheimer), and compare these with the processing workloads imposed by DVS. Specifically, the experiment will monitor the level of perception reached by various patients with attention deficit and/or degenerative diseases when exposed to visual scenes with various levels of complexity; i.e., different shapes and movement patterns of objects and varying lighting and brightness conditions.

It is expected to find similarities between the most complicated situations to perceive by patients and to process by neuromorphic devices. Indeed, differences between both are expected to reveal insights into retinal processing (not implemented in the SONY-Prophesee IMX636 DVS), and potentially guide the design of the algorithms and RTL designs discussed in subsection III.A.

Finally, this axis will continue developing the NA mathematic formalism, which has been proposed by BCAM to map symbolic computations (i.e., computer programs) to biologically plausible neuronal networks [14]. For example, the NA can parsimoniously map a Universal Turing Machine

(a general-purpose computer program) to a neural network with some 200 hard-wired neural units. To date NA has only been proven to map programs and data to artificial recurrent neural networks. SiliconBurmuin will extend NA to map programs/data to biologically plausible SNNs with applications to visual processing.

The NA implementation is a particular instance of Vector Symbolic Architectures (VSAs) [21], which performs Gödel encoding of a computer program and data (in symbolic space) and then employs algebraic representation theory to represent this information as a neural network (in vectorial space). It relies on the fact that very sparse binary representation vectors in high-dimensional Hilbert space ( $n > 100$  M) are likely orthogonal, which eases the implementation of powerful representation theorems for vector symbolic architectures that have already been proven successful for infinite-dimensional Hilbert spaces [22]. In the NA framework, any kind of symbolic computation can be represented by piecewise affine linear transformations acting on highly restricted domains of representation space. A sparse encoding of such binary representation vectors by spike patterns in high-dimensional SNNs would potentially lead to completely new neuromorphic architectures for symbolic computation. Furthermore, since the NA will map symbols and computations onto SNN activation functions, synapses and topologies, then it might help design a theoretical principle for investigating the representation of computations in brain regions and decode the neural code to some extent.

Expected outcomes of this axis include: (1) an API to ease access and control of novel multimodal neuromorphic sensors motivated by neuroscientific observations in sensory topographic maps; (2) an experiment-driven collaboration framework between engineers, clinical researchers and neuroscientists involving the development of a common understanding, knowledge and tools to support cross-disciplinary research; and (3) an NA-based compiler that maps computer programs and data to SNNs that can run on neuromorphic devices.

### C. Semiconductor Axis

The main objective of this axis is to build semiconductor design capabilities in the Basque Country to ensure manufacturability of the SiliconBurmuin RTL designs – including those discussed in subsection III.A. We plan to run several tapeouts (using affordable Europractice process nodes) to refine and optimize the designs for silicon implementation. The longer-term goal is to prove sufficient maturity and open commercialization opportunities (via IP licensing). This effort will be technically led by UPV/EHU and IKERLAN in collaboration with NimbleAI silicon partners, and will be administratively managed by BMH according to the strategy defined by the Spanish PERTE Chip and EU's Chips Act. In a first stage, a RISC-V-powered SoC testchip with testability features will be manufactured using UMC 65-nm process node. The SoC will include interfaces to integrate, validate and characterize simple RTL blocks. In a next stage, the latter blocks will be replaced with neuromorphic IP previously validated in FPGA.

#### D. Industry Axis

This axis is aimed at building strong links between SiliconBurmuin and the (Basque) industry in two directions. First, capture relevant industry requirements to be addressed when designing the neuromorphic IP discussed in subsections III.A and III.B. Secondly, demonstrate the competitive advantages of neuromorphic technology to industry and promote its adoption in new products. The long-term expectation is that SiliconBurmuin IP will eventually power industry products as it becomes mature and is used in new generations of commercial neuromorphic devices. The initial focus is on the railway industry, where CAF is facing the challenge of designing more powerful and safer vision perception systems to deliver better-than-human safety in autonomous trains [4].

As discussed in subsection III.A, SiliconBurmuin is expected to help achieve this objective by proving the feasibility of multimodal DVS-based sensing that potentially unlocks 3D and hyperspectral perception, with extremely low reaction times (already reported for DVS [23]) and reliable performance in adverse weather conditions (already reported for hyperspectral vision [24], [25]). Multimodal datasets enriched with neuromorphic sensing data will be generated to enable this research. The datasets will cover representative driving situations and environmental conditions, and will be adapted to capture limitations imposed by the sensing technology under study. These datasets are expected to provide highly granular ground truth data and hence new insights to overcome current barriers.

#### IV. MAIN TAKEAWAYS

The Basque Government-backed SiliconBurmuin initiative brings together neuroscience, engineering, mathematics and neurology research centres to start a multidisciplinary community capable of fostering innovation in neuromorphic IP design, and ultimately develop the Basque Country as a key player in the rapidly-growing AI hardware technology sector. Notably, the project will study the feasibility of designing the first-ever hyperspectral DVS sensor and subsequent processing pipelines, as well as develop the novel NA mathematic formalism to map computer programs onto SNNs. The later SNNs and the resulting SiliconBurmuin IP will be analyzed using adapted modelling techniques from computational neuroscience to unveil interesting functioning properties that might well inherently develop as part of their biological plausibility, such as retinotopy. SiliconBurmuin shares coordination with the ongoing NimbleAI Horizon Europe project, which is expected to set an adequate technological context for flourishing the Basque neurocomputing community.

The SiliconBurmuin IP will be prototyped on an FPGA together with IP provided by NimbleAI partners, including commercial-grade neuromorphic IP and designs in early phases of development. Once proven feasible and useful, the SiliconBurmuin IP will be validated on a 65-nm testchip. Hence, SiliconBurmuin will also serve to train semiconductor design skills in the Basque Country, in line with the goals set by the Spanish PERTE Chip and EU's Chips Act.

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